List of Reference Attached

1. J. H. Zhao, US patent No. 6,107,649 entitled *Field-controlled high-power semiconductor devices.*

2. K. Asano et al. in IEEE ISPSD-2002, pp.61-64, entitled *5kV 4H-SiC SEJFET with low RonS of 69mΩcm^2.*

3. R. R. Siergiej et al., US patent No. 5,903,020, entitled *Silicon Carbide static induction transistor structure.*

4. J. Nishizawa et al. in IEEE Transactions on Electron Devices, Vol.4, No. 2, Feb. 2000, pp. 482-487, entitled *The 2.45 GHz 36 W CW Si recessed gate type SIT with high gain and high voltage operation.*

5. H. Onose, et al. in Materials Science Forum, Vols.389-393, 2002, pp.1227-1230, entitled *2kV 4H-SiC junction FETs.*

6. J. H. Zhao et al., in IEEE ISPSD-2003, pp.50-52, entitled *3.6 mΩcm^2, 1,726V 4H-SiC normally-off trenched-and-implanted vertical JFETs.*

7. J. H. Zhao et al., in IEE Electronics Letters, Vol.39, No.3, Feb. 6, 2003, pp.321-323 entitled *demonstration of a high performance 4H-SiC vertical junction field effect transistor without epitaxial regrowth.*

List of Drawings Attached

Fig.1 shows prior art in the design of SiCVJFETs.

Fig.2 shows prior art in the design of SiC VJFETs.

Fig.3 shows prior art in the design of SiC static induction transistors (SITs).

Fig.4 shows prior art in another design of SiC static induction transistors (SITs).

Fig.5 shows prior art in yet another design of SiC static induction transistors (SITs).

Fig.6 shows prior art in the design of Si SITs.

Fig.7 shows prior art in the design of long vertical channel and high voltage SiC VJFETs.

Fig.8 shows cross sectional view embodying one form of the invention.

Fig.9 shows cross sectional view of formation of a long vertical channel with a highly uniform channel opening dimension by titled ion implantation of acceptors using thick and heavily doped n^{++} source layer by a self-aligned process.

Fig.10 shows cross sectional view embodying another form of the invention.

Fig.11 shows the cross sectional view of a 4H-SiC VJFET designed and fabricated according to the invention using a single $7x10^{15}cm^{-3}$ doped n-type layer for the drift layer as well as the vertical channel n layer.

Fig.12 shows the experimental room temperature I-V curves for the fabricated 4H-SiC VJFET.

Fig.13 shows the cross sectional view of a design for a 14kV SiC VJFET.

Fig.14 shows the simulated I-V curves for the 14kV SiC VJFET designed.